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10/798,641	03/10/2004	Sean S. Eilert	P18373	6692

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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,641	EILERT, SEAN S.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. **The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.** (emphasis added)

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in

upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Further, the disclosure is objected to because of the following informalities:

- Page 6 line 6: The phrase "may then erased" appears.
- Page 6 line 28: The phrase "and changes as fall" appears.

Appropriate correction is required.

Claim Objections

Claims 2-10, 16-19, and 21-25, are objected to because of the following informalities:

- Dependent claims 12-14 and 27-31 maintain a 'comma' after the claim number from which it depends, wherein the claims noted supra in the objection heading do not. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims **26-31** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As instantly claimed, claim 26 is drawn to software. The Examiner notes that claim 26 can be implemented through the use of a software application, which is non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-6**, **11**, **14-15**, **17-19**, and **26-31** are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (U.S. 6,449,625) hereinafter referred to as Wang.

As per independent claim **1**, Wang teaches,

- A stack configured in a nonvolatile memory to store parameter values (Column 1 lines 48-51).

As per dependent claim **2**, Wang teaches,

- The stack of claim 1 wherein the nonvolatile memory includes a pair of blocks that are erased independently (Column 2 lines 30-34). *The Examiner notes that the inherent characteristic of a stack is that the blocks are able to be erased – independently. Accordingly, Wang teaches the instant limitation with the recitation of stack and its characteristics.*

As per dependent claim **3**, Wang teaches,

- The stack of claim 2 wherein valid parameter values are stored in a first block of the pair of blocks and a second block is erased (Column 2 lines 33-46). *The Examiner notes that the process of garbage collection on the stack provides for the erasure of blocks as instantly claimed.*

As per dependent claim **4**, Wang teaches,

- The stack of claim 3 wherein valid parameter values are stored in the second block of the pair of blocks and the first block is erased (Column 2 lines 33-46). *The Examiner notes that with respect to the comments made supra in claim 3, the garbage collection process is able to identify blocks that are 'stale.' As such, the first block of the non-volatile memory can contain blocks that will be erased as shown in Figures 5A-5F.*

As per dependent claim **5**, Wang teaches,

- The stack of claim 1 further including a register to store an offset value used to generate an address for words in the nonvolatile memory (Column 4 lines 39-41). *The Examiner notes that use of numerically addressable blocks within the nonvolatile memory allows for the operation of a stack to be realized. As taught in Column 4 lines 15-26, the flash memory logs all transactions. Accordingly, the use of addressable blocks and the act of keeping a log of all transactions, teaches the instant limitation of a register used to store values.*

As per dependent claim **6**, Wang teaches,

- The stack of claim 1 further including a smart stack controller to dynamically determine a number of blocks used in the stack (Column 3 lines 25-39).

As per independent claim **11**, Wang teaches,

- A nonvolatile stack to store parameter values in words of a nonvolatile memory (Column 1 lines 48-51).

As per dependent claim **14**, Wang teaches,

- The nonvolatile stack of claim 11, wherein the nonvolatile memory maps a received address to determine memory blocks to be written (Column 4 lines 26-47).

As per independent claim **15**, Wang teaches,

- A storage device, comprising: a nonvolatile memory having multiple blocks in a dynamic block swapped architecture, wherein a pair of blocks are configured to provide a first stack that stores parameter values (Column 1 lines 48-51).

As per dependent claim **17**, Wang teaches,

- The storage device of claim 15 further including a smart stack controller to dynamically determine which blocks from the multiple blocks are used in the first stack (Column 3 lines 25-39).

As per dependent claim **18**, Wang teaches,

- The storage device of claim 15 wherein a second pair of blocks are instantiated in the storage device to configure a second stack (Column 2 lines 30-33).

As per dependent claim **19**, Wang teaches,

- The storage device of claim 15 wherein multiple stacks are instantiated in the storage device with two blocks shared among the multiple stacks (Column 4 lines 61-67).

As per independent claim **26**, Wang teaches,

- A method comprising: configuring a stack in first and second blocks of a nonvolatile memory; and pushing data onto the stack (Column 1 lines 48-51). *The Examiner notes that after Wang has set up the stack in the non-*

volatile memory, the stack has data pushed onto it as shown in Column 4 lines 39-42.

As per dependent claim **27**, Wang teaches,

- The method of claim 26, further including: receiving an address from a processor that is translated by the nonvolatile memory to an address location for storing parameter values in the first and second blocks (Column 4 lines 27-38).

As per dependent claim **28**, Wang teaches,

- The method of claim 26, further including: writing data to a second memory block of the nonvolatile memory when a first memory block is full (Column 4 lines 39-42).

As per dependent claim **29**, Wang teaches,

- The method of claim 28, further including: erasing the first memory block when the data stored in the first memory block is entirely invalid (Column 4 lines 48-60). *The Examiner notes that the process of garbage collection removes the 'invalid' stale blocks as they are blocks that have not been updated recently. Accordingly, the first memory block is erased during the garbage collection cycle as data pushed onto the stack is more recent.*

As per dependent claim **30**, Wang teaches,

- The method of claim 26, further including: scanning for a last valid data entry by confining searches to one memory block for a last stored value within the nonvolatile memory (Column 4 lines 52-55).

As per dependent claim **31**, Wang teaches,

- The method of claim 26, further including: reading the data at an address determined based on register contents and a processor-supplied address (Column 4 liens 27-38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **7**, **12-13**, and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Jou et al (U.S. 5,568,423) hereinafter referred to as Jou.

As per dependent claim **7**, Wang teaches the limitations of independent claim 1 from which dependent claim 7 depends upon as noted supra.

Wang fails to explicitly teach the use of a smart stack controller for the purpose of distributing write cycles.

Jou teach, further including a smart stack controller to distribute write cycles across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou). *The Examiner notes herein that the algorithm used in Jou to evenly distribute the write cycles anticipates the instant limitation of a smart stack controller.*

Wang and Jou are analogous art because they are from the same field of endeavor, namely FLASH memory devices.

At the time of invention it would have been obvious to one of even rudimentary skill in the art, having both the teachings of Wang and Jou before him/her, to combine the algorithm of Jou into Wang for the benefit of guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks.

The suggestion for doing so would have been that, "the wear leveling system of the present disclosure, will operate to guarantee that the usage of each and ever block within the flash memory address space will be equally utilized or fairly distributed (Column 2 lines 27-31 of Jou).

Therefore, it would have been obvious to combine Wang with Jou for the benefit of guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks to obtain the invention as specified in claims 7, 12-13, and 16.

As per dependent claim **12**, the combination of Wang and Jou teach,

- The nonvolatile stack of claim 11, wherein a memory pool in at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification (Column 2 lines 20-48 of Jou).

As per dependent claim **13**, the combination of Wang and Jou teach,

- The nonvolatile stack of claim 11, further including a stack controller to distribute write cycles across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou).

As per dependent claim **16**, the combination of Wang and Jou teach,

- The storage device of claim 15 further including a smart stack controller to distribute write cycles across the multiple blocks (Column 2 lines 20-48 of Jou).

Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view Royer JR et al (U.S. 2003/0061436), hereinafter referred to as Royer.

As per dependent claim **8**, Wang teaches the limitations of independent claim 1 from which dependent claim 8 depends upon as noted supra.

Wang fails to teach, the nonvolatile memory includes polymer memory devices.

Royer teach, the nonvolatile memory includes polymer memory devices (Paragraph 0015).

Wang and Royer are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang and Royer before him/her, to implement the non-volatile memory of Wang in polymer memory devices because polymer memory devices are easy to manufacture, provide a large capacity non-volatile memory array, and are also inexpensive.

The motivation for doing so would have been that, "they are simpler to manufacture, as well as denser in populations. This provides a large capacity, nonvolatile memory array that is not very expensive (Paragraph 0016 of Royer)."

Therefore it would have been obvious to combine Wang with Royer for the benefit of a easy to manufacture, large capacity non-volatile memory array that is inexpensive, to obtain the invention as specified in claim 8.

Claims **9-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Lucker et al (U.S. 2005/0114588), hereinafter referred to as Lucker, with Royer JR et al (U.S. 2003/0061436), hereinafter referred to as Royer, used as evidentiary support.

As per dependent claim **9**, Wang teaches the limitations of independent claim 1 from which dependent claim 9 depends upon as noted supra.

Wang fails to teach, the polymer memory devices are plastic memory devices.

Lucker teach, the polymer memory devices are plastic memory devices (Paragraph 0059).

Wang, Lucker, and Royer are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang, Lucker, and Royer before him/her, to implement the non-volatile memory of Wang in plastic polymer memory devices because polymer memory devices are easy to manufacture, provide a large capacity non-volatile memory array, and are also inexpensive.

The motivation for doing so would have been that, "they are simpler to manufacture, as well as denser in populations. This provides a large capacity, nonvolatile memory array that is not very expensive (Paragraph 0016 of Royer)."

Therefore it would have been obvious to combine Wang with Lucker for the benefit of a easy to manufacture, large capacity non-volatile memory array that is inexpensive, to obtain the invention as specified in claims 9 and 10.

As per dependent claim **10**, Lucker teach,

- The stack of claim 8 wherein the polymer memory devices are resistive change polymer memory devices (Paragrah 0059).

Claims **20-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Lipsanen et al (U.S. 2004/0242203) hereinafter referred to as Lipsanen.

As per independent claim **20**, Wang teaches, and a nonvolatile memory coupled to the processor to provide a nonvolatile stack to store parameter values (Column 1 lines 48-51).

Wang does not teach, a computer system, comprising: first and second antennas; a transceiver coupled to the first and second antennas; a processor coupled to the transceiver.

Lipsanen teach, first and second antennas; a transceiver coupled to the first and second antennas; a processor coupled to the transceiver (Paragraph 0049 of Lipsanen as shown in Figure 2).

Wang and Lipsanen are from the same field of endeavor, namely computing systems.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang and Lipsanen before him/her, to combine the

computing system taught by Lipsanen with the flash memory stack of Wang for the benefit of having a flash memory stack in the non-volatile memory of Lipsanen so as not to shorten the life of the memory unit.

The motivation for doing so would have been that, "the flash memory is rated for a limited number of write cycles, and so frequent database updates can shorten the life of the flash memory unit. The invention addresses these and other problems (Column 1 lines 22-24 of Wang)."

Therefore it would have been obvious to combine Wang with Lipsanen for the benefit of a stack in the memory unit of Lipsanen to obtain the invention as specified in claims 20-22.

As per dependent claim **21**, the combination of Wang and Lipsanen teach,

- The computer system of claim 20 wherein the nonvolatile memory includes first and second blocks that are configured to form the nonvolatile stack and are erased independently (Column 2 lines 30-34 of Wang). *The Examiner notes that the inherent characteristic of a stack is that the blocks are able to be erased – independently. Accordingly, Wang teaches the instant limitation with the recitation of stack and its characteristics.*

As per dependent claim **22**, the combination of Wang and Lipsanen teach,

- The computer system of claim 20 further including a register to store an offset value used to generate an address for words in the nonvolatile memory (Column 4 lines 39-41 of Wang). *The Examiner notes that use of numerically addressable blocks within the nonvolatile memory allows for*

the operation of a stack to be realized. As taught in Column 4 lines 15-26, the flash memory logs all transactions. Accordingly, the use of addressable blocks and the act of keeping a log of all transactions, teaches the instant limitation of a register used to store values.

Claim **23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Lipsanen and in further view of Royer JR et al (U.S. 2003/0061436), hereinafter referred to as Royer.

As per dependent claim **23**, the combination of Wang and Lipsanen teaches the limitations of independent claim 20 from which dependent claim 23 depends upon as noted supra.

The combination of Wang and Lipsanen fails to teach, where the nonvolatile stack includes polymer memory devices.

Royer teach, where the nonvolatile stack includes polymer memory devices (Paragraph 0015).

The combination of Wang and Lipsanen, and Royer are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang, Lipsanen, and Royer before him/her, to implement the non-volatile memory of Wang in polymer memory devices because polymer memory devices are easy to manufacture, provide a large capacity non-volatile memory array, and are also inexpensive.

The motivation for doing so would have been that, "they are simpler to manufacture, as well as denser in populations. This provides a large capacity, nonvolatile memory array that is not very expensive (Paragraph 0016 of Royer)."

Therefore it would have been obvious to combine Wang and Lipsanen with Royer for the benefit of a easy to manufacture, large capacity non-volatile memory array that is inexpensive, to obtain the invention as specified in claim 23.

Claim **24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Lipsanen and in further view of Ovshinsky et al (U.S. 5,296,716), hereinafter referred to as Ovshinsky.

As per dependent claim **24**, the combination of Wang and Lipsanen teaches the limitations of independent claim 20 from which dependent claim 24 depends upon as noted supra.

The combination of Wang and Lipsanen fails to teach, where the nonvolatile stack includes Chalcogenide memory devices.

Ovshinsky teach, where the nonvolatile stack includes Chalcogenide memory devices (Column 5 lines 17-20).

The combination of Wang and Lipsanen, and Ovshinsky are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang, Lipsanen, and Ovshinsky before him/her, to implement the non-volatile memory of Wang in Chalcogenide memory devices because Chalcogenide memory devices operate faster at lower energy levels.

The motivation for doing so would have been that, "... chalcogenide memory materials in a unique configurations, which memory materials exhibit orders of magnitude higher switching speeds at remarkably reduced energy levels (Column 5 lines 16-20 of Ovshinsky)."

Therefore it would have been obvious to combine Wang and Lipsanen with Ovshinsky for the benefit memory devices that operate faster at lower energy levels to obtain the invention as specified in claim 24.

Claim **25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Lipsanen and in further view of Nakos et al (U.S. 6,054,745), hereinafter referred to as Nakos.

As per dependent claim **25**, the combination of Wang and Lipsanen teaches the limitations of independent claim 20 from which dependent claim 25 depends upon as noted supra.

The combination of Wang and Lipsanen fails to teach, where the nonvolatile stack includes microelectromechanical (MEM) memory devices.

Nakos teach, where the nonvolatile stack includes microelectromechanical (MEM) memory devices (Column 1 lines 5-10).

The combination of Wang and Lipsanen, and Nakosare analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Wang, Lipsanen, and Nakos before him/her, to implement the non-volatile memory of Wang in microelectromechanical memory devices

(MEM) because MEM memory devices have faster write times conventional nonvolatile memory cells.

The motivation for doing so would have been that, "it is a further object of the present invention to provide a nonvolatile memory cell which has faster write times (Column 2 lines 11-13 of Nakos)."

Therefore it would have been obvious to combine Wang and Lipsanen with Nakos for the benefit memory devices that have faster write times to obtain the invention as specified in claim 25.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. U.S. 7,000,071 Ciesinger et al teach a method for virtually enlarging, or reconfiguring, the flash memory, non-volatile, stack of a portable data carrier.

2. U.S. 6,820,197 Benedix et al teach a stack configured in a non-volatile memory to store data.

3. U.S. 2003/0167373 Winters et al teach a stack configured in a non-volatile memory to store data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb

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SUPERVISORY PATENT EXAMINER